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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/693,491

10/27/2003

Shunpei Yamazaki

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26171

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EXAMINER

BROCK II, PAUL E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/693,491

Applicant(s)

YAMAZAKI ET AL.

Examiner

Paul E Brock II

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6, 25 and 26 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 25 and 26 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 10/105,282.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 8-20-04.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3, 5, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa et al. (JPPAT 2001-035808, Suzawa) in view of Hibino et al. (JP 2001-010685, Hibino).

With regard to claim 1, Suzawa discloses in figure 12 a semiconductor device. Suzawa discloses in figures 6 and 12 a semiconductor layer (601 in figure 6) over an insulating surface (102 in figure 12). Suzawa discloses in figures 6 and 12 a gate insulating film (602 in figure 6) on said semiconductor layer. Suzawa discloses in figures 6 and 12 a gate electrode (118 – 123 in figure 12 and 603b and 604b in figure 6) on said gate insulating film. Suzawa discloses in figures 6 and 12 wherein said semiconductor layer comprises a channel formation region (206, 210, 214, 218, 222, or 228 in figure 12), at least one LDD region (207, 211, 215, 219, 223, or 229 in figure 12) in contact with said channel formation region, and a source region (208, 213, 216, 221, or 225 in figure 12) or a drain region (209, 212, 217, or 220 in figure 12) in contact with said LDD region. Suzawa discloses in figures 6 and 12 wherein said gate electrode has a taper shape. Suzawa discloses in figures 6 and 12 wherein said gate electrode comprises a laminate of a fourth electrode (603b in figure 6) and a fifth electrode (604b in figure 6). Suzawa does not teach

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wherein said gate electrode comprises a laminate of a fourth electrode, a fifth electrode and a sixth electrode. Hibino teaches in figure 3b a gate electrode (12) having a taper shape wherein the gate electrode comprises a laminate of a fourth electrode (13), a fifth electrode (14) and a sixth electrode (15). It would have been obvious to one of ordinary skill in the art at the time of the present invention to form the three layered gate electrode of Hibino in the device of Suzawa in order to prevent erosion of the gate electrode during formation of the device as stated by the English language translation of Hibino (USPAT 6529251) in column 3, lines 14 – 18 (a more specific application of why this is true can be found in column 6, lines 27 – 29 and 39 – 43, as well as column 7, lines 38 – 45).

With regard to claim 3, Suzawa teaches in paragraphs [0011] that fourth and fifth electrode layers at the top and bottom of a gate stack can comprise W or Ti. Hibino discloses in paragraphs 68 – 69 wherein top and bottom electrode layers in a gate stack comprise Ti, and a middle gate stack layer comprises Al. Therefore, it would have been further obvious in the method of Suzawa and Hibino wherein the fourth conductive film is a conductive film comprising W or a material including W as its main component, the fifth conductive film is a conductive film comprising Al or a material including Al as its main component and the sixth conductive film is a conductive film comprising Ti or a material including Ti as its main Component.

With regard to claim 5, Suzawa discloses in figure 12 said fourth electrode is overlapped with said LDD region through said gate insulating film.

With regard to claim 25, Suzawa discloses in figure 18a wherein said semiconductor device is selected from the group consisting of a computer.

3. Claims 2, 4, 6, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa in view of Yudasaka et al. (USPAT 5953582, Yudasaka) and Hibino et al. (JP 2001-010685, Hibino).

With regard to claim 2, Suzawa discloses in figure 12 a semiconductor device. Suzawa discloses in figures 6 and 12 a semiconductor layer (601 in figure 6) over an insulating surface (102 in figure 12). Suzawa discloses in figures 6 and 12 a gate insulating film (602 in figure 6) on said semiconductor layer. Suzawa discloses in figures 6 and 12 a gate electrode (118 – 123 in figure 12 and 603b and 604b in figure 6) on said gate insulating film. Suzawa discloses in figures 6 and 12 wherein said semiconductor layer comprises a channel formation region (206, 210, 214, 218, 222, or 228 in figure 12), at least one LDD region (207, 211, 215, 219, 223, or 229 in figure 12) in contact with said channel formation region, and a source region (208, 213, 216, 221, or 225 in figure 12) or a drain region (209, 212, 217, or 220 in figure 12) in contact with said LDD region. Suzawa is silent to the impurity concentrations of the LDD, source and drain regions. Yudasaka teaches in figure 26 and column 26, lines 8 – 15 wherein an LDD region (642b) comprises a impurity region for giving one conductivity at a concentration of 1×10^{17} to $1 \times 10^{20} \text{ cm}^{-3}$, and one of said source region (642a) and said drain region (643a) comprises said impurity element at a concentration of 1×10^{20} to $1 \times 10^{21} \text{ cm}^{-3}$ (the disclosed ranges of 3×10^{18} to $1 \times 10^{19} \text{ cm}^{-3}$ and $1 \times 10^{20} \text{ cm}^{-3}$ make the claimed range obvious, see MPEP 2144.05 I). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the impurity concentrations of Yudasaka in the method of Suzawa in order to use an impurity concentration that is well known in the art for LDD and source/drain regions, respectively.

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Suzawa discloses in figures 6 and 12 wherein said gate electrode has a taper shape. Suzawa discloses in figures 6 and 12 wherein said gate electrode comprises a laminate of a fourth electrode (603b in figure 6) and a fifth electrode (604b in figure 6). Suzawa and Yudasaka do not teach wherein said gate electrode comprises a laminate of a fourth electrode, a fifth electrode and a sixth electrode. Hibino teaches in figure 3b a gate electrode (12) having a taper shape wherein the gate electrode comprises a laminate of a fourth electrode (13), a fifth electrode (14) and a sixth electrode (15). It would have been obvious to one of ordinary skill in the art at the time of the present invention to form the three layered gate electrode of Hibino in the device of Suzawa and Yudasaka in order to prevent erosion of the gate electrode during formation of the device as stated by the English language translation of Hibino (USPAT 6529251) in column 3, lines 14 – 18 (a more specific application of why this is true can be found in column 6, lines 27 – 29 and 39 – 43, as well as column 7, lines 38 – 45).

With regard to claim 4, Suzawa teaches in paragraphs [0011] that fourth and fifth electrode layers at the top and bottom of a gate stack can comprise W or Ti. Hibino discloses in paragraphs 68 – 69 wherein top and bottom electrode layers in a gate stack comprise Ti, and a middle gate stack layer comprises Al. Therefore, it would have been further obvious in the method of Suzawa and Hibino wherein the fourth conductive film is a conductive film comprising W or a material including W as its main component, the fifth conductive film is a conductive film comprising Al or a material including Al as its main component and the sixth conductive film is a conductive film comprising Ti or a material including Ti as its main Component.

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With regard to claim 6, Suzawa discloses in figure 12 said fourth electrode is overlapped with said LDD region through said gate insulating film.

With regard to claim 26, Suzawa discloses in figure 18a wherein said semiconductor device is selected from the group consisting of a computer.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1 – 6 , 25, and 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3, and 7 of U.S. Patent No. 6,657,260 in view of Yudasaka. Claims 1, 3, and 7 teach all of the claim limitations of Yudasaka, but fail to specifically teach a channel formation region, an LDD region, source/drain regions, and that the gate electrode has a tapered structure. Yudasaka provides teaching for these features and the reasons for combination are obvious to one of ordinary skill similar to the 103 rejections above.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ono et al., and Suzawa (EP '124) both disclose tapered gate shapes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II

A handwritten signature in black ink, appearing to read "Paul E Brock II", with a stylized flourish at the end.